# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S51 | 12 | (verifi$6 verify$3 validat$3 test$3 "logic checking" logic$1checking (co adj verifi$6) co$1verifi$6 (co adj verify$3) co$1verify$3 (co adj validat$3) co$1validat$3) SAME (satisfiability SAT) SAME (BMC "bounded model checking" bounded$1model$1checking) SAME (loop looped looping iteration iterate iterating iterated iterative feedback feed$1back) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 17:25 |
| S50 | 2 | (verifi$6 verify$3 validat$3 test$3 "logic checking" logic$1checking (co adj verifi$6) co$1verifi$6 (co adj verify$3) co$1verify$3 (co adj validat$3) co$1validat$3) WITH (satisfiability SAT) WITH (BMC "bounded model checking" bounded$1model$1checking) WITH (loop looped looping iteration iterate iterating iterated iterative feedback feed$1back) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 17:25 |
| S49 | 5 | ((design model abstraction abstract abstracting abstracted circuit system Dynamic) with (verifi$6 verify$3 validat$3 test$3 "logic checking" logic$1checking (co adj verifi$6) co$1verifi$6 (co adj verify$3) co$1verify$3 (co adj validat$3) co$1validat$3)) AND (unroll unrolled unrolling un$1roll un$1rolled un$1rolling) SAME (satisfiability SAT) AND Lazy | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 17:25 |
| S52 | 7 | Aarti.in. Gupta.in. Malay.in. Ganai.in. Zijiang.in. Yang.in. Pranav.in. Ashar.in. | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | AND | ON | 2008/02/11 17:27 |
| S54 | 7 | (S49 S50 S51 S52 S53) AND diver | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 17:29 |
| S53 | 7 | (Gupta.in. Ganai.in. Yang.in. Ashar.in.) AND diver AND (satisfiability SAT) AND (BMC "bounded model checking" bounded$1model$1checking) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 17:29 |
| S58 | 3 | (S49 S50 S51 S52 S53) AND ((external outside outward outer) ADJ2 (constraint assertion checker declaration affirmation "hooked up" forced defined restriction "boolean expression" "logical expression" condition)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 18:03 |
| S57 | 2 | (S49 S50 S51 S52 S53) AND ((interface interfaced interfacing connection connecting connect connected link linked linking linkage boundary boundaries interaction interactions interacted terminal ) ADJ2 (constraint assertion checker declaration affirmation "hooked up" forced defined restriction "boolean expression" "logical expression" condition)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 18:03 |
| S56 | 18 | (S49 S50 S51 S52 S53) AND (((design model circuit) with (abstract abstracted abstraction abstracting reduce reduced reducing reduction decrease decreased decreasing shrink shrinking shrunk condense condensed condensing compress compressed compressing compression contract contracted contracting simplify simplified simplifying simplification drop dropped dropping transform transformed transforming transformation))) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 18:03 |

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|---|---|---|---|---|---|---|
| S55 | 3 | (S49 S50 S51 S52 S53) AND (Lazy WITH (constraint assertion checker declaration affirmation "hooked up" forced defined restriction "boolean expression" "logical expression" condition)) | US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2008/02/11 18:03 |

http://www.google.com/
"DIVER: SAT-based model checking platform for verifying large scale systems"
"Formal Verification in an Industrial Setting: DiVer Verification Platform White Paper"
"Formal Verification in an Industrial Setting: DiVer Verification Platform"
"Formal Verification in an Industrial Setting" DiVer Verification Platform
Formal Verification Industrial Setting DiVer Verification Platform
Ashar Ganai Gupta Yang Formal Verification Industrial Setting DiVer Verification Platform
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"Improved SAT-based Bounded Reachability Analysis,"